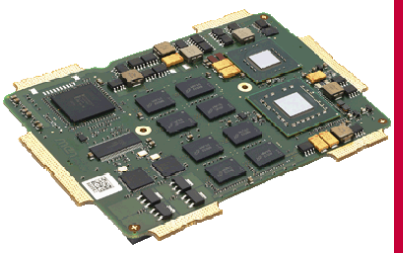
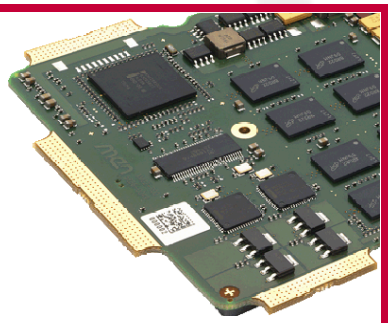
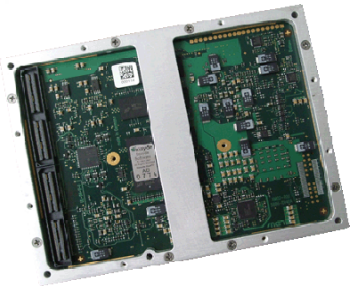
User Manual

XM2 - ESMexpress® COM with Intel® Core™ 2 Duo



Module without cover and frame





Module inside cover and frame

XM2 - ESMexpress® COM with Intel® Core™ 2 Duo

The XM2 is a Computer-On-Module which together with an application-specific carrier board forms a semi-custom solution for industrial, harsh, mobile and mission-critical environments.

The XM2 is controlled by a Intel® Core™ 2 Duo CPU with a clock frequency of up to 2.26 GHz and a total power consumption of up to 40W.

The XM2 can accommodate 4 GB of DDR3 DRAM memory and supports other memory like USB Flash on the carrier board.

The GS45 graphics controller supports x16 PCI Express® Graphics or up to two SDVO interfaces, or one LVDS port.

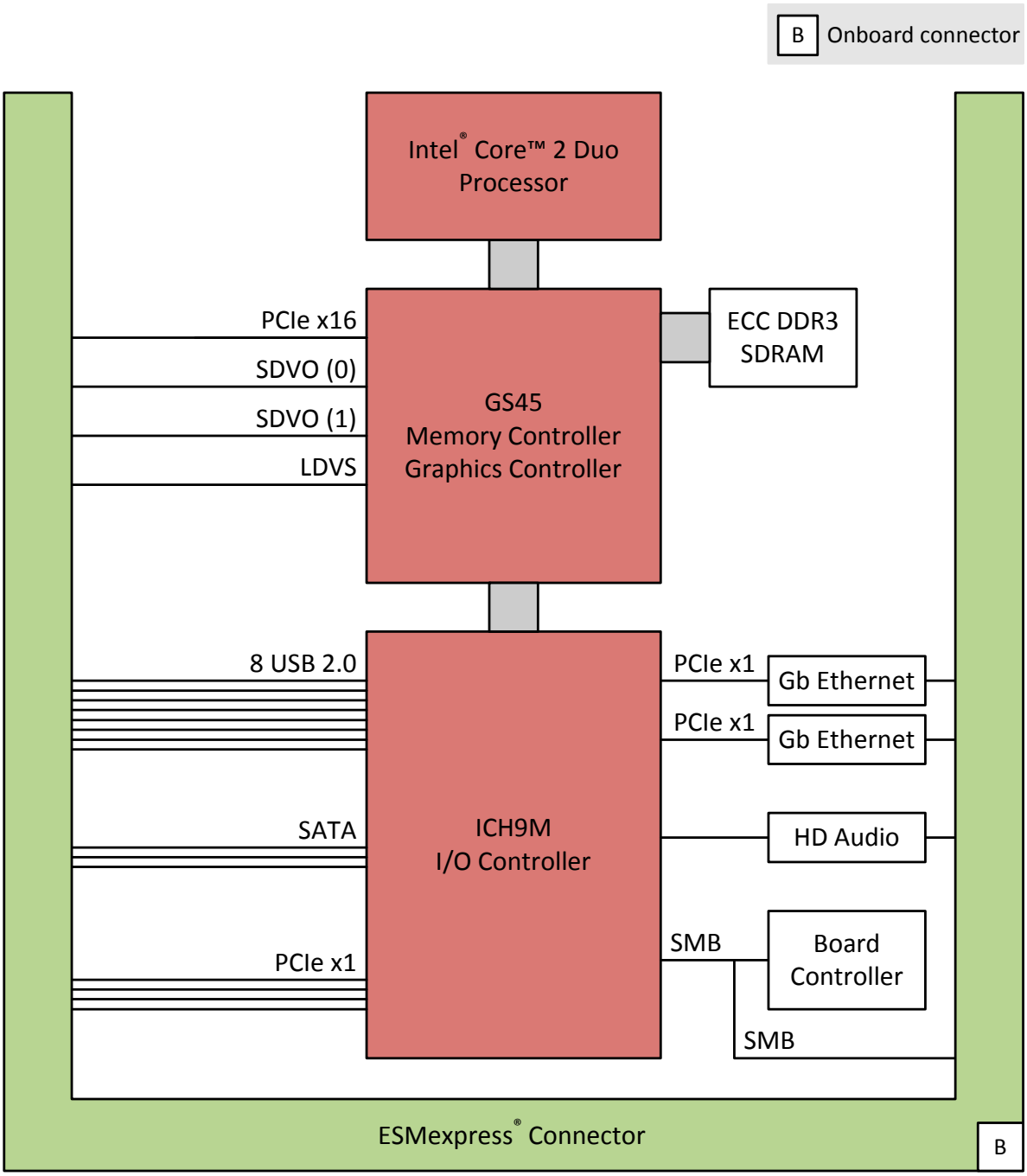
In addition, four x1 or one x4 PCI Express® links are supported by the XM2. Other modern serial interfaces are 2 Gigabit Ethernet channels, 8 USB ports, 3 SATA ports, and one HD audio port. These interfaces are all routed from the XM2 for availability on any ESMexpress® carrier board.

The XM2 is completed by a board management controller for temperature and power supervision. It comes with an InsydeH2O™ EFI BIOS configurable for the final application.

The XM2 is screened for operation from 0°C to +85°C (Tcase). As all ESMexpress® modules it is embedded in a covered frame. This ensures EMC protection and allows efficient conductive cooling. Air cooling is also possible by applying a heat sink on top of the cover. With a low power processor the module may even be operated in an extended temperature range. ESMexpress® modules are firmly screwed to a carrier board and come with rugged industry-proven connectors supporting high frequency and differential signals. Only soldered components are used to withstand shock and vibration, and the design is optimized for conformal coating. All ESMexpress® modules support a single 95x125mm form factor.

For evaluation and development purposes an ATX carrier board is available. The ESMexpress® module can be evaluated on a COM Express® carrier board via an adapter from ESMexpress® to COM Express®.

Diagram


B Onboard connector
Intel® Core™ 2 Duo Processor
PCIe x16
SDVO (0)
SDVO (1)
LDVS
GS45 Memory Controller Graphics Controller
ECC DDR3 SDRAM
8 USB 2.0
SATA
PCIe x1
ICH9M I/O Controller
PCIe x1
Gb Ethernet
PCIe x1
Gb Ethernet
HD Audio
SMB
Board Controller
SMB
ESMexpress® Connector
B

Technical Data

CPU

- Intel® Core™ 2 Duo SP9300
  - Up to 2.26GHz processor core frequency
  - 800/1066MHz system bus frequency
- Chipset
  - Northbridge: Intel® GS45
  - Southbridge: Intel® ICH9M-E

Memory

- Up to 6MB L2 cache integrated in Core 2 Duo
- Up to 4GB DDR3 SDRAM system memory
  - Soldered
  - 800/1067MHz memory bus frequency locked to the FSB frequency

Serial ATA (SATA)

- Three ports via ESMexpress® connector
- Transfer rates up to 3Gbit/s (SATA 3.0)

Graphics

- Integrated in Intel® GS45 chipset
- Maximum resolution: 2048 Þ 1536 pixels (QXGA)
- One x16 link (PCI Express® graphics) or
- Up to two SDVO ports
- One LVDS port (4 bit, max. 1366x768)
- Available via ESMexpress® connector

USB

- Eight USB 2.0 host ports
- UHCI implementation
- Data rates up to 480Mbit/s
- Available via ESMexpress® connector

Ethernet

- Two 10/100/1000Base-T Ethernet channels
- Ethernet controllers connected by two x1 PCIe® links
- Two LED signals per channel for LAN link, activity status and connection speed
- Available via ESMexpress® connector

PCI Express®

- Two x1 links to connect local 1000Base-T Ethernet controllers
- Four x1 links or one x4 link via ESMexpress® connector (switchable on the carrier)
- Data rate 250MB/s in each direction (2.5 Gbit/s per lane)

GPIO

- 1 line from PIC via ESMexpress® connector
- Usable for LED

HD audio

- Via ESMexpress® connector

Board Management Controller

- Input voltage supervision
- Power sequencing
- Board monitoring
- Watchdog
- Accessible via SMBus

Miscellaneous

- Real-time clock (with GoldCap or battery backup on the carrier board)
- SMBus interface

Electrical Specifications

- Supply voltage/power consumption:
  - +12V (-25%/+33%), power consumption up to 40W
  - +5V (-5%/+5%) standby voltage

Mechanical Specifications

- Dimensions: 95mm x 125mm
- ESMexpress® PCB mounted between a frame and a cover
- Weight: 230g (incl. cover and frame)

Environmental Specifications

- Temperature range (operation): 0..+85°C Tcase (ESMexpress® cover/frame) (screened)
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms (EN 60068-2-27)
- Bump: 10g/16ms (EN 60068-2-29)
- Vibration (sinusoidal): 1g/10..150Hz (EN 60068-2-6)
- Conformal coating on request

MTBF

- 154,077h @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC

- EMC behavior depends on the system and housing surrounding the ESMexpress® module.
- MEN has performed general, successful EMC tests for ESMexpress® using the XC1 evaluation carrier according to:
  - EN 55022 (radio disturbance)
  - IEC 61000-4-2 (ESD)
  - IEC 61000-4-3 (electromagnetic field immunity)
  - IEC 61000-4-4 (burst)
  - IEC 61000-4-5 (surge)
  - IEC 61000-4-6 (conducted disturbances)

BIOS

- InsydeH2O™ UEFI Framework

Software Support

- Windows® (Windows® XP, Windows® 7)
- Linux
  - tested/verified with: Ubuntu 10.04 (kernel 2.6.32-21) 32-bit and 64-bit versions
  - OpenSuse 11.3 32-bit and 64-bit versions
  - and: CentOS 5.5 (kernel 2.6.18) 32-bit and 64-bit versions
  - Detailed matrix of supported interfaces under Ubuntu 10.04 and OpenSuse 11.3
- VxWorks® (in preparation)
- QNX®
- For more information on supported operating system versions and drivers see online data sheet.

Configuration Options

CPU

- Intel® SP9300, 2.26GHz, 1066MHz FSB, 6MB cache, 25W
- Intel® SL9400, 1.86GHz, 1066MHz FSB, 6MB cache, 17W
- Intel® SU9300, 1.2GHz, 800MHz FSB, 3MB cache, 10W
- Intel® Celeron® M722, 1.2GHz, 800MHz FSB, 1MB cache, 5.5W
- Intel® Celeron® M723, 1.2GHz, 800MHz FSB, 1MB cache, 10W

Memory

- System RAM
  - 1 GB, 2GB or 4GB

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

For available standard configurations see online data sheet.

Product Safety

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual is intended only for system developers and integrators, it is not intended for end users.

It describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Issue	Comments	Date
E1	First issue	2009-09-30
E2	Update of BIOS description - Invalid! Changes reversed in E3	2011-03-04
E3	Changed EMC information in Technical Data Removed DisplayPort and HDMI references Removed all ANSI-VITA 59 references	2014-02-21

Conventions

This sign marks important notes or warnings concerning the use of voltages which can lead to serious damage to your health and also cause damage or destruction of the component.

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics — Folder, file and function names are printed in *italics*.

bold — **Bold** type is used for emphasis.

`monospace` — A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

comment — Comments embedded into coding examples are shown in green color.

hyperlink — Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ#
/IRQ — Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out — Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous issue of the document.

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Since July 1, 2006 all MEN standard products comply with RoHS legislation.

Since January 2005 the SMD and manual soldering processes at MEN have already been completely lead-free. Between June 2004 and June 30, 2006 MEN's selected component suppliers have changed delivery to RoHS-compliant parts. During this period any change and status was traceable through the MEN ERP system and the boards gradually became RoHS-compliant.

WEEE Application

The WEEE directive does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company which puts the product on the market, as defined in the directive; components and sub-assemblies are not subject to product compliance.

In other words: Since MEN does not deliver ready-made products to end users, the WEEE directive is not applicable for MEN. Users are nevertheless recommended to properly recycle all electronic boards which have passed their life cycle.

Nevertheless, MEN is registered as a manufacturer in Germany. The registration number can be provided on request.

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1 Getting Started

This chapter gives an overview of the board and some hints for first installation in a system.

1.1 Map of the Board

The following board map shows the board assembly from its cover side (top) and connector side (bottom). The cover includes holes for mounting the ESMexpress module onto a COM Express carrier.

Figure 1. *Map of the board – cover side*

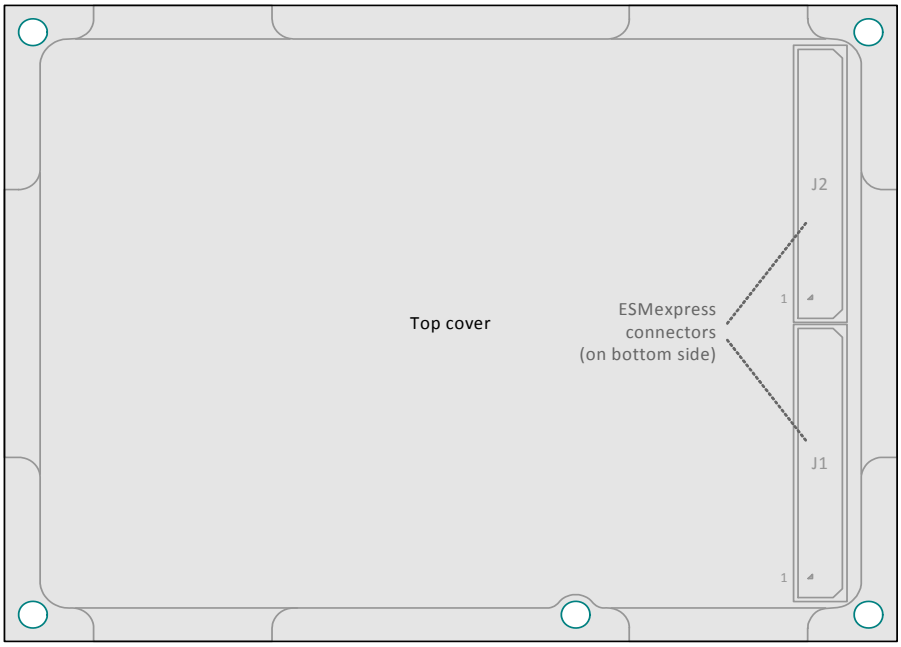
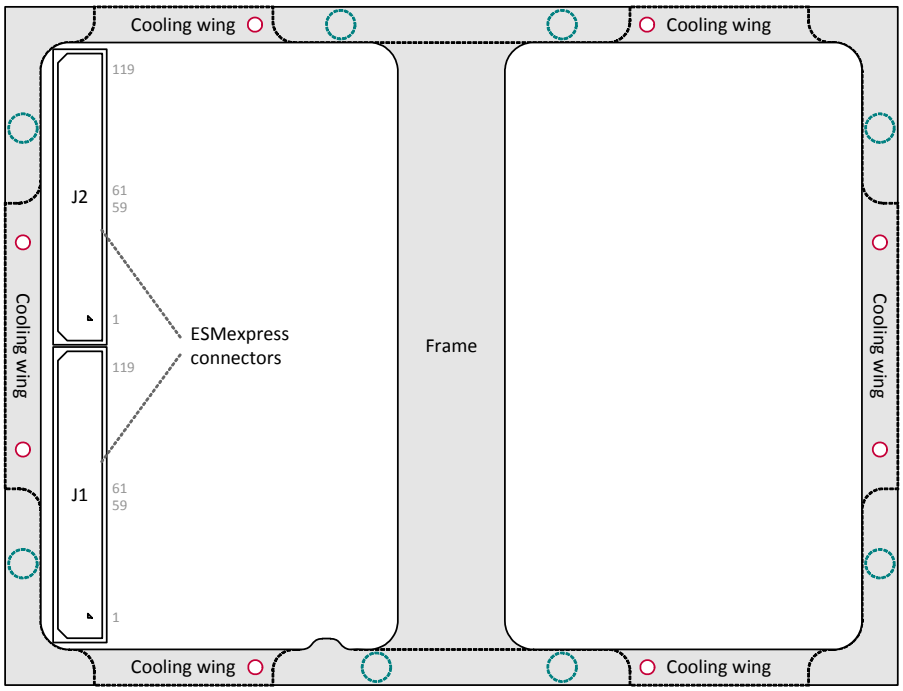


Figure 2. *Map of the board – connector side*



1.2 First Operation

You can use the following check list when installing the board for the first time and with minimum configuration using a Windows host PC.

- ☑ Power-down the system.
- ☑ Install the XM2 on your ESMexpress carrier board, making sure that the ESMexpress connectors are properly aligned.

To provide a better example, we assume that you are using MEN's standard evaluation carrier, XC1, which provides the necessary connections. You can find more information on the XC1 in the XC1 User Manual, which is available for download on MEN's website.

- ☑ Connect a USB keyboard and mouse to the USB connectors of the XC1.
- ☑ Connect a flat-panel display to the DVI connector of the XC1.
- ☑ Power-up the system.
- ☑ You can start up the BIOS setup menu by hitting the <F2> key (see Chapter 3 BIOS on page 41).
- ☑ Now you can make configurations in BIOS (see Chapter 3 BIOS on page 41).
- ☑ Observe the installation instructions for the respective software.

1.3 Installing Operating System Software

The board supports Windows, Linux, VxWorks and QNX.

By standard, no operating system is installed on the board. Please refer to the operating system installation documentation on how to install the software!

You can find any software available on MEN's website.

1.3.1 Installing Windows 2000 via USB

If you want to install Windows 2000 using a USB CD-ROM drive, you must install from a Windows 2000 CD including Service Pack 4 to avoid problems. This is a known Windows problem.

1.4 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

You can find any driver software available for download on MEN's website.

2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned (Chapter 5.1 Literature and Web Resources on page 78).

2.1 Power Supply

The XM2 board is supplied with +12V (9..16V) only.

The XM2 board can optionally be supplied with +5V (±5%) standby voltage. This voltage can be used for the Wake-on-LAN functionality, for example.

All other required voltages are generated onboard.

2.2 Board Supervision

The XM2 provides an intelligent board management controller (BMC) with the following main features:

- Board power sequencing control
- Voltage supervision
- System watchdog
- Software reset functionality
- Error state logging
- Power mode settings
- SMBus communication with main CPU

The watchdog device monitors the board on operating system level. If enabled, the watchdog must be triggered by application software. If the trigger is overdue, the watchdog initiates a board reset and this way can put the system back into operation when the software hangs.

The watchdog uses a configurable time interval or is disabled. Settings are made through BIOS or via an MEN software driver.

In addition, the XM2 uses a National LM95245 device to measure the CPU die temperature and the local board temperature.

MEN provides dedicated software drivers for the board controller and LM95245 device. For a detailed description of the functionality of the driver software please refer to the drivers' documentation.

You can find any driver software and documentation available for download on MEN's website.

2.3 Reset

The XM2 generates its own reset signal. You can wake it up from reset state by externally switching the power supply off and on.

2.4 Real-Time Clock

The supply voltage for the RTC should be buffered with an external Goldcap or battery device mounted on the carrier board.

2.5 Processor Core

The XM2 can be equipped with different types of Intel Core 2 Duo or Celeron processors. The following table gives a performance overview:

Table 1. *Processor core options on XM2*

Processor Type	Core Frequency	Power Class	L2 Cache	Front Side Bus
Intel Core 2 Duo SP9300	2.26 GHz	25 W	6 MB	1066 MHz
Intel Core 2 Duo SL9400	1.86 GHz	17W	6 MB	1066 MHz
Intel Core 2 Duo SU9300	1.2 GHz	10 W	3 MB	800 MHz
Intel Celeron M722	1.2GHz	5.5 W	1 MB	800 MHz
Intel Celeron M723	1.2 GHz	10 W	1 MB	800 MHz

2.5.1 Thermal Considerations

The XM2 has a power dissipation of up to 40W.

The ESMexpress module is enclosed inside a cover and frame and therefore provides a flexible thermal interface that can be used as needed to fulfill the thermal needs of the application. Typically you should use it for conduction cooling or convection cooling. It depends on the system configuration and airflow if an additional heat sink is needed or not. In any case you should check your thermal conditions and implement appropriate cooling.

See also Chapter 2.14.2 Thermal Concept on page 25.

Please note that if you do not use the cover and frame supplied by MEN and/or no heat sink, warranty on functionality and reliability of the XM2 may cease. If you have any questions or problems regarding thermal behavior, please contact MEN.

2.6 Memory

2.6.1 DRAM System Memory

The board provides up to 4 GB on-board, soldered DDR3 SDRAM. The memory bus is 2x64 bits wide (dual channel) and operates with up to 1067 MHz.

The XM2 supports memory down technology. The memory is not realized with complete modules. Instead single memory chips with a maximum of 2 Gbit per chip are used.

2.6.2 Boot Flash

The XM2 has an 16-Mbit SPI Flash implemented as on-board Flash for BIOS data.

2.6.3 EEPROM

The board has a 2-kbit serial EEPROM for factory data.

2.7 Mass Storage: Serial ATA (SATA)

The ICH I/O Controller Hub of the XM2 provides three serial ATA channels which are led to the ESMexpress connector.

The SATA interface supports transfer rates up to 3 Gbits/s and RAID 0 or RAID 1 functionality.

You can find the pinout for the SATA signals in Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 29.

2.8 Graphics

The graphics core of the XM2 is part of the GMCH.

It supports a resolution of up to 2048x1536 pixels.

It provides one PCI Express® graphics x16 link, up to two SDVO ports, or one LVDS port.

You can find the pinout for the graphics signals in Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 29 and in Table 5, Pin assignment of ESMexpress connector J2, pins 91..120 on page 31.

2.9 USB Interface

The XM2 provides eight USB 2.0 interfaces at the ESMexpress connector.

They are controlled by four UHCI controllers for USB 1.1 and two EHCI controllers for USB 2.0 in the ICH9M I/O controller.

You can find the pinout for the USB signals in Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 29.

2.10 Ethernet Interface

The XM2 provides two Gigabit Ethernet interfaces at the ESMexpress connector. The Ethernet controllers are connected to the ICH9M I/O controller via two PCI Express x1 links.

The interfaces are controlled by two Intel 82574L Ethernet controllers. They support 10 Mbits/s up to 1000 Mbits/s as well as full-duplex operation, autonegotiation and Wake-on-LAN functionality.

The controllers have their own EEPROM to store the MAC address etc. The Ethernet transformers have to be mounted on the carrier board.

You can find the pinout for the Ethernet signals in Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 30.

The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable. The MAC addresses on XM2 are:

- LAN1: `0x 00 C0 3A 9C Ex xx`
- LAN2: `0x 00 C0 3A 9D Fx xx`

where "00 C0 3A" is the MEN vendor code, "9C" and "9D" are the MEN product codes. The last four digits depend on the interface and the serial number of the product. The serial number is added to the offset, for example for LAN1:

- Serial number 0042: `0x xx xx = 0xE000 + 0x002A = 0x E0 2A.`

(See Chapter 5.2 Finding out the Board's Article Number, Revision and Serial Number on page 79.)

2.10.1 Ethernet Status LEDs

The XM2 provides two status LEDs for each Ethernet channel. They signal the link and activity and can be led to the carrier board via the ESMexpress connectors.

See Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 30.

2.11 Audio

The XM2 supports a high definition audio interface on the ESMexpress connector.

The ICH9M I/O controller, however, only includes the controller. If you want to use audio you have to implement an external codec on a carrier board.

You can find the pinout for the audio signals in Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 30.

2.12 Status LED

The XM2 provides one GPIO pin driven by the board controller for a board status LED. The line cannot be used as input.

The LED can be made available on the carrier board. It is switched on when the BIOS starts, switched off when the board is switched off and flashing when the board is in stand-by (S3) status.

During normal operation the LED can be switched on and off via the MEN driver for the board controller. See MEN's website for further information.

In case of a board failure, the LED displays the following error messages:

Table 2. *Error codes signaled by board management controller via LED flashes*

Number of Flashes	Error	Description
1	XM02BCI_ERR_33A	External 3.3 V failure
2	XM02BCI_ERR_INP	Input voltage failure
3	XM02BCI_ERR_NO_EXT_PWR_OK	External power supply failure
4	XM02BCI_ERR_ICH_HANDSHAKE	Chipset handshake failure
5	XM02BCI_ERR_NO_DDRVR_PWRGD	Memory voltage failure
6	XM02BCI_ERR_NO_PWRGD_5130	1.05 V or internal 3.3 V voltage failure
7	XM02BCI_ERR_NO_IMVP_PWRGD	CPU voltage failure
8	XM02BCI_ERR_NO_GFX_PWRGD	Graphic voltage failure
9	XM02BCI_ERR_PLT_RST_TIMEOUT	Platform reset timeout
10	XM02BCI_ERR_CPU_RST_TIMEOUT	CPU Reset timeout
11	XM02BCI_ERR_BIOS_TIMEOUT	BIOS timeout
12	XM02BCI_ERR_CPU_TOO_HOT	CPU too hot
255	CPUBCI_INVALID_MAIN_STATE	Invalid PIC main state

You can find the GPIO/LED pin in Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 30.

2.13 PCI Express Interface

The ICH9M I/O controller provides up to six PCI Express x1 links. Each link supports 2.5GB/s bandwidth in each direction.

Four x1 or one x4 ports can be accessed on the ESMexpress connector, the other two are used for the Ethernet interfaces.

The GS45 graphics controller provides an additional PCIe x16 graphics root port (PEG). This root port supports up to 40GB/s bandwidth in each direction. See Chapter 2.8 Graphics on page 22.

You can find the pinout for the PCI Express signals on the ESMexpress connector in Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 29, Table 5, Pin assignment of ESMexpress connector J2, pins 91..120 on page 31, Table 6, Pin assignment of ESMexpress connector J2, pins 61..90 on page 32 and Table 7, Pin assignment of ESMexpress connector J2, pins 1..60 on page 33.

2.14 ESMexpress

ESMexpress is a Computer-On-Module (COM/SOM) standard that is especially ruggedized and provides a high-performance, low-power architecture for harsh environments.

The ESMexpress concept has been developed for applications that require highly robust electronics to ensure safe and reliable operation even in severe environments, e.g., in railways and avionics, industrial automation and medical engineering or mobile applications in general.

Together with an application-specific carrier board, it forms a semi-custom solution for industrial, harsh, mobile and mission-critical environments.

2.14.1 Mechanical Concept

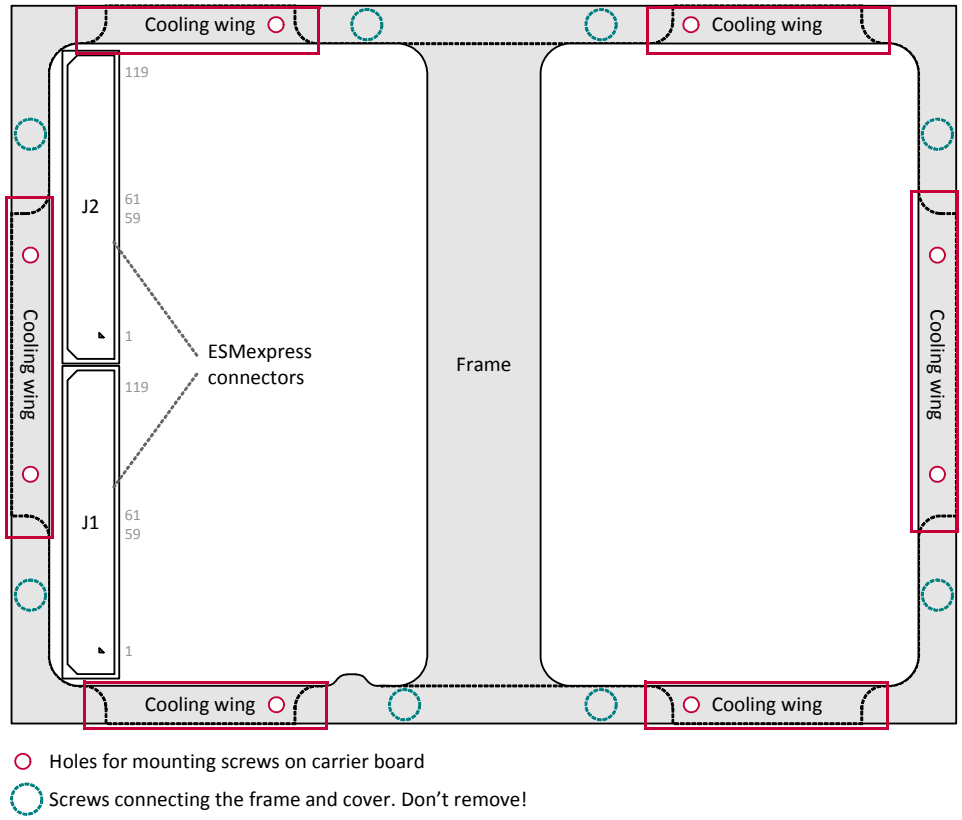
ESMexpress modules are embedded in a frame and a cover, and are firmly screwed to a carrier board. The frame and the cover ensure 100% EMC protection. Only soldered components are used to withstand shock and vibration, and the design is optimized for conformal coating. All ESMexpress modules support a single 95 x 125 mm form factor.

2.14.2 Thermal Concept

ESMexpress modules are equipped with eight cooling wings for conductive cooling. The heat generated on the board is transported to the frame and the cover via the cooling wings. The frame and the cover, however, are only part of the thermal solution for a module. They only provide a common interface between the ESMexpress module and implementation-specific thermal solutions.

The module can e.g. be cooled via conductive cooling, where the heat is transported to a housing or a heat sink built on top of the cover. Where operating temperatures are moderate, the module may even do without the frame and cover, with a suitable low-power processor and airflow.

Figure 3. *ESMexpress thermal concept: cooling wings between frame and cover*



Please contact MEN's sales team for further information.

2.14.3 ESMexpress Connectors

The XM2 is connected to the carrier board via two 120-pin connectors.

Connector types:

- 2-row, 120-pin high-speed receptacle, 0.5mm pitch, e.g. Samtec QSH-060-01-L-D-A-K
- Mating connector:
  2-row, 120-pin high-speed plug connector, 0.5mm pitch

Note: In the following pinout tables the ESMexpress connectors are shown as if seen **through** the cover side and PCB, i.e. the pin layout (position of pin 1) will be the same on a carrier board.

Cf. Figure 1, Map of the board – cover side (page 17) and Figure 2, Map of the board – connector side (page 18).

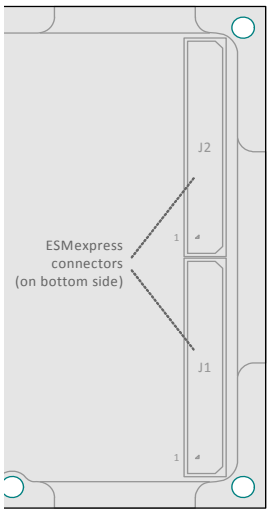
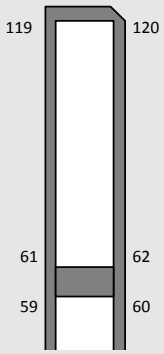
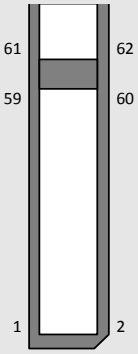


Table 3. *Pin assignment of ESMexpress connector J1, pins 61..120*



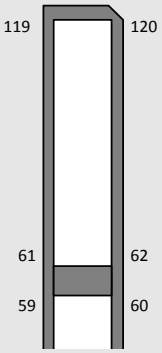
	119	PCIE_A0_TX+	GND	120	PCIE_A0_RX+
	117	PCIE_A0_TX-		118	PCIE_A0_RX-
	115	GND		116	GND
	113	PCIE_CLK_A0_REF+		114	LVDS_CLK+
	111	PCIE_CLK_A0_REF-		112	LVDS_CLK-
	109	GND		110	GND
	107	LVDS0+		108	LVDS1+
	105	LVDS0-		106	LVDS1-
	103	LVDS2+		104	LVDS3+
	101	LVDS2-		102	LVDS3-
	99	L_DDC_CLK		100	L_DDC_DATA
	97	GND		98	GND
	95	SATA0_TX+		96	SATA0_RX+
	93	SATA0_TX-		94	SATA0_RX-
	91	GND		92	GND
	89	SATA1_TX+		90	SATA1_RX+
	87	SATA1_TX-		88	SATA1_RX-
	85	GND		86	GND
	83	SATA2_TX+		84	SATA2_RX+
	81	SATA2_TX-		82	SATA2_RX-
	79	GND		80	GND
	77	USB0+		78	USB1+
	75	USB0-		76	USB1-
	73	USB_OC_0_1#		74	USB_OC_2_3#
	71	USB2+		72	USB3+
	69	USB2-		70	USB3-
	67	GND		68	GND
	65	USB4+		66	USB5+
	63	USB4-		64	USB5-
	61	USB_OC_4_5#		62	USB_OC_6_7#

Table 4. *Pin assignment of ESMexpress connector J1, pins 1..60*



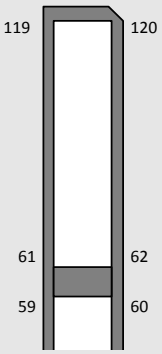
59	USB6+		60	USB7+
57	USB6-		58	USB7-
55	Vbatt		56	+5VSB
53	PWR_OK		54	PS_ON#
51	SMB_DATA		52	RESET_IN#
49	SMB_CLK		50	RESET_OUT#
47	SMB_ALERT#		48	WAKE#
45	GPIO/LED		46	PWRBTN#
43	HDA_IO		44	-
41	HDA_SYNC		42	-
39	HDA_BIT_CLK		40	HDA_SDIN
37	HDA_RST#		38	HDA_SDOUT
35	-		36	-
33	-		34	-
31	-		32	-
29	-	+12V	30	-
27	-		28	-
25	-		26	GND
23	ETH_B_LED_LINK#		24	ETH_B_LED_ACT#
21	ETH_B0+		22	ETH_B1+
19	ETH_B0-		20	ETH_B1-
17	ETH_B2+		18	ETH_B3+
15	ETH_B2-		16	ETH_B3-
13	ETH_B_REF		14	GND
11	ETH_A_LED_LINK#		12	ETH_A_LED_ACT#
9	ETH_A0+		10	ETH_A1+
7	ETH_A0-		8	ETH_A1-
5	ETH_A2+		6	ETH_A3+
3	ETH_A2-		4	ETH_A3-
1	ETH_A_REF		2	GND

Table 5. *Pin assignment of ESMexpress connector J2, pins 91..120*



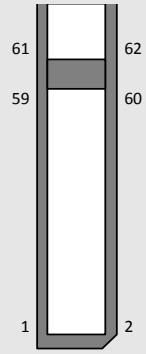
	119	PCIE_B0_TX+/ SDVOB_RED+		120	PCIE_B0_RX+/ SDVO_TVCLKIN+
	117	PCIE_B0_TX-/ SDVOB_RED-		118	PCIE_B0_RX-/SDVO_T-VCLKIN-
	115	GND		116	GND
	113	PCIE_B1_TX+/ SDVOB_GREEN+		114	PCIE_B1_RX+/ SDVOB_INT+
	111	PCIE_B1_TX-/ SDVOB_GREEN-		112	PCIE_B1_RX-/ SDVOB_INT-
	109	GND		110	GND
	107	PCIE_B2_TX+/ SDVOB_BLUE+		108	PCIE_B2_RX+/SDVO_-FLDSTALL+
	105	PCIE_B2_TX-/ SDVOB_BLUE-	GND	106	PCIE_B2_RX-/SDVO_-FLDSTALL-
	103	GND		104	GND
	101	PCIE_B3_TX+/ SDVOB_CLK+		102	PCIE_B3_RX+
	99	PCIE_B3_TX-/SDVOB_-CLK-		100	PCIE_B3_RX-
	97	GND		98	GND
	95	PCIE4_TX+/ SDVOC_RED+		96	PCIE_B4_RX+
	93	PCIE4_TX-/ SDVOC_RED-		94	PCIE_B4_RX-
	91	GND		92	GND

Table 6. *Pin assignment of ESMexpress connector J2, pins 61..90*



89	PCIE_B5_TX+/ SDVOC_GREEN+		90	PCIE_B5_RX+/ SDVOC_INT+
87	PCIE_B5_TX-/ SDVOC_GREEN-		88	PCIE_B5_RX-/ SDVOC_INT-
85	GND		86	GND
83	PCIE_B6_TX+/ SDVOC_BLUE+		84	PCIE_B6_RX+
81	PCIE_B6_TX-/ SDVOC_BLUE-		82	PCIE_B6_RX-
79	GND		80	GND
77	PCIE_B7_TX+/ SDVOC_CLK+	GND	78	PCIE_B7_RX+
75	PCIE_B7_TX-/SDVOC_-CLK-		76	PCIE_B7_RX-
73	GND		74	GND
71	PCIE_B8_TX+		72	PCIE_B8_RX+
69	PCIE_B8_TX-		70	PCIE_B8_RX-
67	GND		68	GND
65	PCIE_B9_TX+		66	PCIE_B9_RX+
63	PCIE_B9_TX-		64	PCIE_B9_RX-
61	DDPC_CTRLDATA		62	DDPC_CTRLCLK

Table 7. *Pin assignment of ESMexpress connector J2, pins 1..60*



	59	SDVO_CTRLDATA		60	SDVO_CTRLCLK
	57	PCIE_B10_TX+		58	PCIE_B10_RX+
	55	PCIE_B10_TX-		56	PCIE_B10_RX-
	53	GND		54	GND
	51	PCIE_B11_TX+		52	PCIE_B11_RX+
	49	PCIE_B11_TX-		50	PCIE_B11_RX-
	47	GND		48	GND
	45	PCIE_B12_TX+		46	PCIE_B12_RX+
	43	PCIE_B12_TX-		44	PCIE_B12_RX-
	41	GND		42	GND
	39	PCIE_B13_TX+		40	PCIE_B13_RX+
	37	PCIE_B13_TX-		38	PCIE_B13_RX-
	35	GND		36	GND
	33	PCIE_B14_TX+		34	PCIE_B14_RX+
	31	PCIE_B14_TX-	GND	32	PCIE_B14_RX-
	29	GND		30	GND
	27	PCIE_B15_TX+		28	PCIE_B15_RX+
	25	PCIE_B15_TX-		26	PCIE_B15_RX-
	23	GND		24	CLK_REQ_CLK_B_REF#
	21	PCIE_CLK_A1_REF+		22	PCIE_CLK_B_REF+
	19	PCIE_CLK_A1_REF-		20	PCIE_CLK_B_REF-
	17	CLK_REQ_CLK_A1_REF#		18	GND
	15	PCIE_A3_TX+		16	PCIE_A3_RX+
	13	PCIE_A3_TX-		14	PCIE_A3_RX-
	11	GND		12	GND
	9	PCIE_A2_TX+		10	PCIE_A2_RX+
	7	PCIE_A2_TX-		8	PCIE_A2_RX-
	5	GND		6	GND
	3	PCIE_A1_TX+		4	PCIE_A1_RX+
	1	PCIE_A1_TX-		2	PCIE_A1_RX-

Table 8. *Signal mnemonics of 120-pin ESMexpress connectors*

	Signal	Direction	Function
Power	+5VSB		5V standby voltage
	GND	-	Ground
	Vbatt		3V battery voltage
Power Management	PCIE_WAKE#	in	Wake signal from PCIe device to wake XM2 from sleep state
	PS_ON#	out	Enable signal for external power supply
	PWRBTN#	in	Power button
	PWR_OK	in	Power OK signal from external power supply
	RESET_IN#	in	Reset signal from carrier board
	RESET_OUT#	out	Reset signal from CPU board
PCI Express	PCIE_CLK_A0_REF+, PCIE_CLK_A0_REF-	out	Reference clock A0 100 MHz
	CLK_REQ_CLK_A0_REF#	in	100 MHz clock request signal A0
	PCIE_CLK_A1_REF+, PCIE_CLK_A1_REF-	out	Reference clock A1 100 MHz
	CLK_REQ_CLK_A1_REF#	in	100 MHz clock request signal A1
	PCIE_CLK_B_REF+, PCIE_-CLK_B_REF-	out	Reference clock B 100 MHz
	CLK_REQ_CLK_B_REF#	in	100 MHz clock request signal B
	PCIE_A0_RX+, PCIE_A0_RX-	in	Differential PCIe receive lines, lane 0
	PCIE_A0_TX+, PCIE_A0_TX-	out	Differential PCIe transmit lines, lane 0
	PCIE_A1_RX+, PCIE_A1_RX-	in	Differential PCIe receive lines, lane 1
	PCIE_A1_TX+, PCIE_A1_TX-	out	Differential PCIe transmit lines, lane 1
	PCIE_A2_RX+, PCIE_A2_RX-	in	Differential PCIe receive lines, lane 2
	PCIE_A2_TX+, PCIE_A2_TX-	out	Differential PCIe transmit lines, lane 2
	PCIE_A3_RX+, PCIE_A3_RX-	in	Differential PCIe receive lines, lane 3
	PCIE_A3_TX+, PCIE_A3_TX-	out	Differential PCIe transmit lines, lane 3
PCIe-based Graphics Interface Signals	PCIE_B[15:0]_RX+, PCIE_B[15:0]_RX-	in	PCI Express Graphics Receive Differential Pair or regular PCIe 1x16 or 2x8. SDVO and PCI Express Interface for Graphics architecture are muxed together
	PCIE_B[15:0]_TX+, PCIE_B[15:0]_TX-	out	PCI Express Graphics Transmit Differential Pair or regular PCIe 1x16 or 2x8

	Signal	Direction	Function
LVDS	L_DDC_CLK	in/out	EDID support for flat-panel display
	L_DDC_DATA	in/out	EDID support for flat-panel display
	LVDS_CLK+, LVDS_CLK-	out	LVDS differential clock output
	LVDS0-, LVDS0+	out	Differential LVDS lines, port 0
	LVDS1-, LVDS1+	out	Differential LVDS lines, port 1
	LVDS2-, LVDS2+	out	Differential LVDS lines, port 2
	LVDS3-, LVDS3+	out	Differential LVDS lines, port 3
SATA	SATA0_RX+, SATA0_RX-	in	Differential SATA receive lines, port 0
	SATA0_TX+, SATA0_TX-	out	Differential SATA transmit lines, port 0
	SATA1_RX+, SATA1_RX-	in	Differential SATA receive lines, port 1
	SATA1_TX+, SATA1_TX-	out	Differential SATA transmit lines, port 1
	SATA2_RX+, SATA2_RX-	in	Differential SATA receive lines, port 2
	SATA2_TX+, SATA2_TX-	out	Differential SATA transmit lines, port 2
USB	USB0+, USB0-	in/out	Differential USB lines, port 0
	USB1+, USB1-	in/out	Differential USB lines, port 1
	USB2+, USB2-	in/out	Differential USB lines, port 2
	USB3+, USB3-	in/out	Differential USB lines, port 3
	USB4+, USB4-	in/out	Differential USB lines, port 4
	USB5+, USB5-	in/out	Differential USB lines, port 5
	USB6+, USB6-	in/out	Differential USB lines, port 6
	USB7+, USB7-	in/out	Differential USB lines, port 7
	USB_OC_0_1#	in	USB overcurrent, ports 0 and 1
	USB_OC_2_3#	in	USB overcurrent, ports 2 and 3
	USB_OC_4_5#	in	USB overcurrent, ports 4 and 5
	USB_OC_6_7#	in	USB overcurrent, ports 6 and 7
HD Audio	HDA_IO	-	Reference voltage for external HDA codec I/O voltage level
	HDA_BIT_CLK	out	HD audio serial data clock
	HDA_RST#	out	HD audio reset
	HDA_SDIN	in	HD audio serial data in
	HDA_SDOUT	out	HD audio serial data out
	HDA_SYNC	out	HD audio synchronization

	Signal	Direction	Function
Ethernet	ETH_A_LED_ACT#	out	Signal for activity status LED, port A
	ETH_A_LED_LINK#	out	Signal for link status LED, port A
	ETH_A0+, ETH_A0-	in/out	Media Dependent Interface [0] data, differential pair, port A
	ETH_A1+, ETH_A1-	in/out	Media Dependent Interface [1] data, differential pair, port A
	ETH_A2+, ETH_A2-	in/out	Media Dependent Interface [2] data, differential pair, port A
	ETH_A3+, ETH_A3-	in/out	Media Dependent Interface [3] data, differential pair, port A
	ETH_A_REF	out	Port A reference voltage
	ETH_B_LED_ACT#	out	Signal for activity status LED, port B
	ETH_B_LED_LINK#	out	Signal for link status LED, port B
	ETH_B0+, ETH_B0-	in/out	Media Dependent Interface [0] data, differential pair, port B
	ETH_B1+, ETH_B1-	in/out	Media Dependent Interface [1] data, differential pair, port B
	ETH_B2+, ETH_B2-	in/out	Media Dependent Interface [2] data, differential pair, port B
	ETH_B3+, ETH_B3-	in/out	Media Dependent Interface [3] data, differential pair, port B
	ETH_B_REF	out	Port B reference voltage

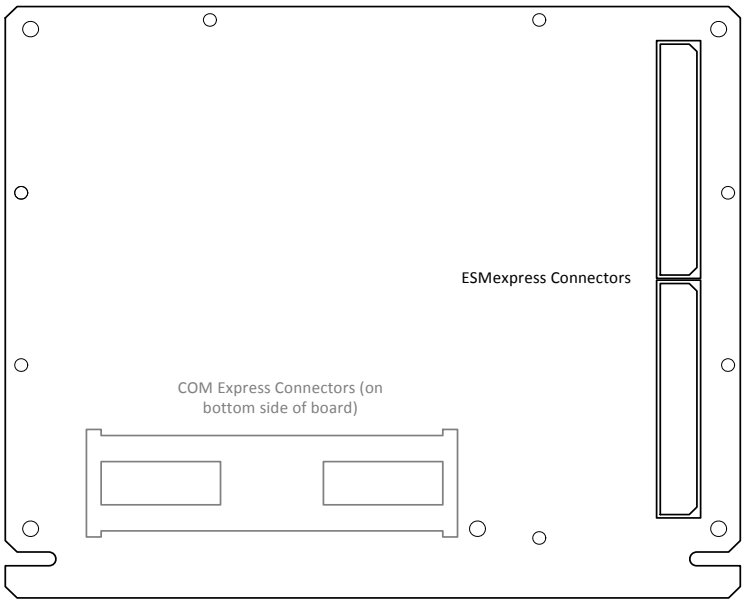
	Signal	Direction	Function
Serial Digital Video Output (SDVO)	SDVOB_BLUE+, SDVOB_BLUE-	out	Serial digital video B blue data, differential pair
	SDVOB_GREEN+, SDVOB_GREEN-	out	Serial digital video B green data, differential pair
	SDVOB_RED+, SDVOB_RED-	out	Serial digital video B red data, differential pair
	SDVOB_CLK+, SDVOB_-CLK-	out	Serial digital video B clock, differential pair
	SDVOB_INT+, SDVOB_INT-	in	Serial digital video B input interrupt, differential pair
	SDVOC_BLUE+, SDVOC_BLUE-	out	Serial digital video B blue data, differential pair
	SDVOC_GREEN+, SDVOC_GREEN-	out	Serial digital video B green data, differential pair
	SDVOC_RED+, SDVOC_RED-	out	Serial digital video B red data, differential pair
	SDVOC_CLK+, SDVOC_-CLK-	out	Serial digital video B clock, differential pair
	SDVOC_INT+, SDVOC_INT-	in	Serial digital video B input interrupt, differential pair
	SDVO_FLDSTALL+, SDVO_-FLDSTALL-	in	Serial digital video field stall, differential pair
	SDVO_TVCLKIN+, SDVO_TVCLKIN-	in	Serial digital video TVOUT synchronization clock, differential pair
	SDVOCTRL_CLK	in/out	I²C based control signal (clock) for SDVO device
	SDVOCTRL_DATA	in/out	I²C based control signal (data) for SDVO device
GMBus	SDVO_CTRLCLK	in/out	I2C-based control signal (clock) for DisplayPort device
	SDVO_CTRLDATA	in/out	I2C-based control signal (data) for DisplayPort device
	DDPC_CTRLCLK	in/out	I2C-based control signal (clock) for SDVO device
	DDPC _CTRLDATA	in/out	I2C-based control signal (data) for SDVO device
Other	SMB_ALERT#	in	SMBus alert
	SMB_CLK	in/out	SMBus clock
	SMB_DATA	in/out	SMBus data
	GPIO/LED	in/out	GPIO line for board status LED

2.14.4 Using an ESMexpress Module on a COM Express Carrier Board

The AE12 adapter card offers the possibility to evaluate an ESMexpress module on a COM Express carrier board. It complies with the COM Express Type 2 basic form factor.

On its top side the AE12 has ESMexpress connectors for connecting the ESMexpress module. On the bottom side the AE12 card is equipped with standard COM Express connectors for plugging it onto the COM Express carrier.

Figure 4. *AE12 COM Express adapter board – Map of the board*

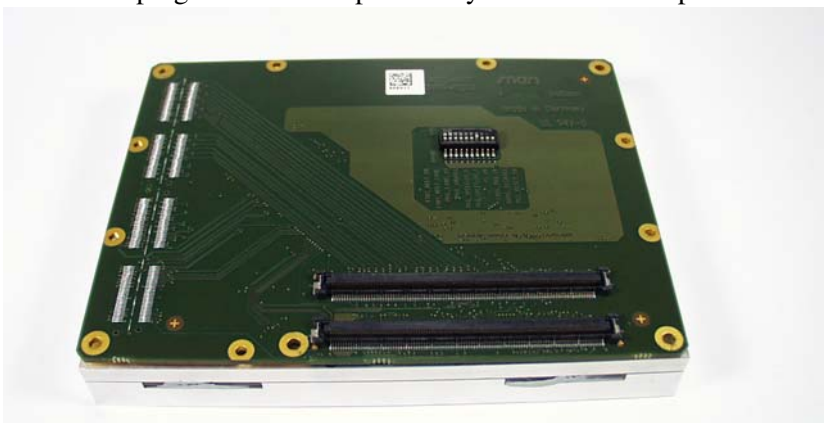


The pin assignment of the COM Express connectors is compliant to the COM Express standard.

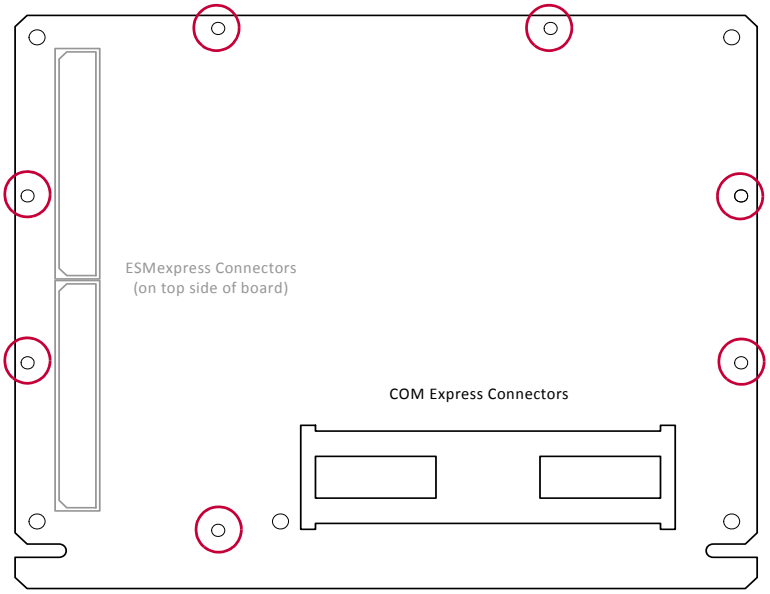
The pin assignment of the ESMexpress connectors is compliant to the ESMexpress standard.

Installing the ESMexpress Module on a COM Express Carrier

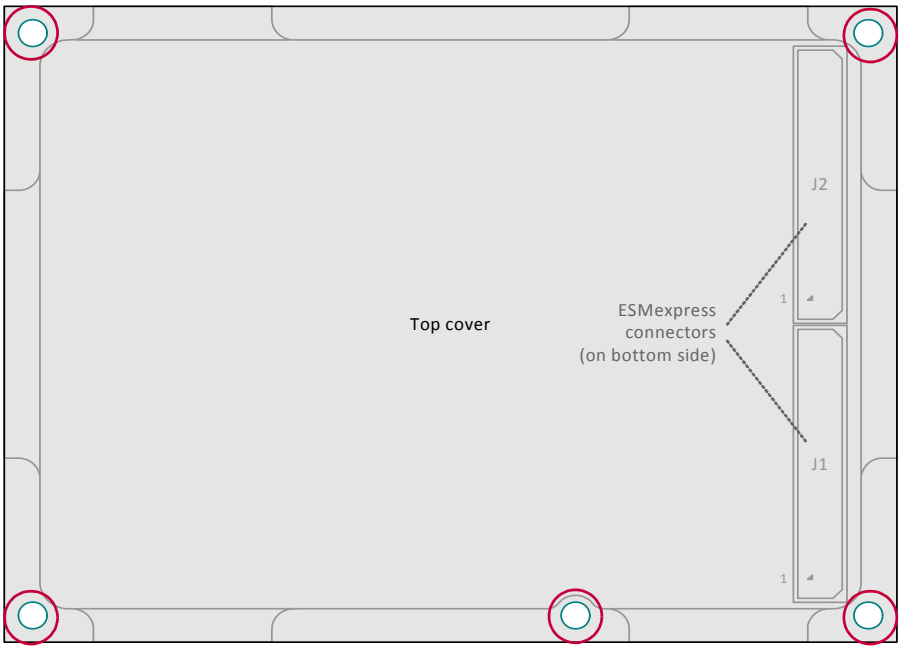
☑ Align the ESMexpress connectors and the mounting holes of the adapter and the module and plug the AE12 adapter firmly onto the ESMexpress module.



☑ Install the ESMexpress module on the adapter using the following mounting holes and the seven M2x4 cross-recess pan-head screws included in the delivery of the adapter:



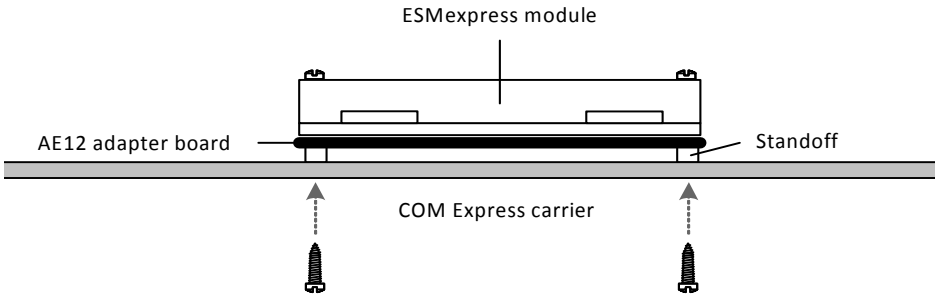
☑ Turn the module around and insert five 2.5x18 cross-recess countersink-head screws (also included in the delivery) into the five COM Express mounting holes on the top of the ESMexpress module.



☑ Install the five 2.5x5 standoffs on the bottom of the adapter.

☑ Plug the ESMexpress module/AE12 assembly onto the COM Express carrier board.

☑ Screw the adapter onto the COM Express carrier board using five M2.5x4 screws.



3 BIOS

The XM2 is equipped with an InsydeH2O setup utility from Insyde Software. InsydeH2O is Insyde Software's firmware product line designed to replace traditional PC BIOS. It is an implementation of the Intel's Platform Innovation Framework for UEFI /EFI. The UEFI/EFI specification defines a new model for the interface between operating systems and platform firmware. This interface consists of data tables that contain platform-related information, plus boot and runtime service calls that are available to the operating system and its loader. Together, these provide a standard environment for booting an operating system and running pre-boot applications. This product line is the next generation of PC BIOS technology.

The ">" character in front of a menu item means that a sub-menu is available. An "x" in front of a menu item means that there is a configuration option which needs to be activated through a higher configuration option before being accessible.

3.1 Main

InsydeH2O Setup Utility					Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit

InsydeH2O Version	XM2 BIOS V 1.xx
Processor Type	Intel Celeron M CPU 722 @ 1.20GHz
System Bus Speed	800MHz
System Memory Speed	800MHz
Cache RAM	1024kB
Total Memory	2048MB
SODIMM 0	1024MB
SODIMM 1	1024MB
Language	<English>
System Time	[hh:mm:ss]
System Date	[mm/dd/yyyy]

F1 Help	↑↓ Select Item	F5/F6 Change Values	F9 Setup Defaults
Esc Exit	← → Select Menu	Enter Select > Sub-menu	F10 Save and Exit

InsydeH2O Version / MEN Board / Processor Type / System Bus Speed / System Memory Speed / Cache RAM/ Total Memory/ SODIMM 0 / SODIMM 1

Description	You cannot change any values in these fields. They are only for information.

Language

Description	Select the default language
Options	*English*

System Time

Description	Change the internal clock.	
Options	*hh*	Hours (Valid range from 0 to 23)
	mm	Minutes (Valid range from 0 to 59)
	ss	Seconds (Valid range from 0 to 59)

System Date

Description	Change the date	
Options	*mm*	Month (Valid range from 1 to 12)
	dd	Day (Valid range from 1 to 31)
	yyyy	Year (Valid range from 2000 to 2099)

3.2 Advanced

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
>Boot Configuration						
>Peripheral Configuration						
>IDE Configuration						
>Video Configuration						
>USB Configuration						
>Chipset Configuration						
>ACPI Table/Features Control						
>PCI Express Root Port 1						
>PCI Express Root Port 2						
>PCI Express Root Port 3						
>PCI Express Root Port 4						
>PCI Express Root Port 5						
>PCI Express Root Port 6						
F1 Help		↑↓ Select Item		F5/F6 Change Values		F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Sub-menu		F10 Save and Exit

Boot Configuration — Sub-menu

```
NumLock                   [On]
Power Supply Type         [AT]
Watchdog                  [Off]
SMI Handler               [On]
PWRON after PWR-Fail      [On]
ATX_PWRGD Failure Mode    [Check at Start-Up]
Spread Spectrum Control   [On]
```

Numlock		
Description	Selects power-on state for Numlock	
Options	*On*	*Off*
Power Supply Type		
Description	Selects the type of power supply	
Options	*AT*	*ATX*
Watchdog		
Description	Enables or disables the XM2 Watchdog	
Options	*Off*	*10 min*
	1 min	*15 min*
	2 min	*20 min*
	5 min	*30 min*
SMI Handler		
Description	Enables or disables the SMI functionality	
Options	*On*	*Off*
PWRON after PWR-Fail		
Description	Sets the system power status when power returns to the system from a power failure situation.	
Options	*On*	*Off*
	Former State	
ATX_PWRGD Failure Mode		
Description	Determines the system behavior in case of a failure at the ATX power good signal	
Options	*Check at Start-Up*	*Check always*
Spread Spectrum Control		
Description	Enable or disable Spread Spectrum	
Options	*On*	Spread Spectrum enabled
	Off	Spread Spectrum disabled

Peripheral Configuration — Sub-menu

```
HD Audio            [Auto]
LAN-1               [On]
LAN-2               [On]
```

HD Audio		
Description	Enable or disable the HD Audio controller.	
Options	*Auto*	The controller is enabled if a codec is found.
	Disabled	The controller is disabled even when there is an audio codec.
	Enabled	The controller is enabled independent of the presence of a codec.
LAN-1/LAN-2		
Description	Enables or disables the LAN interfaces.	
Options	*On*	*Off*

IDE Configuration — Sub-menu

```
IDE Controller           [Enabled]
HDC Configure as         [AHCI]

>Channel 1 Master
>Channel 2 Master
>Channel 3 Master
>Channel 4 Master
```

IDE Controller

Description	Enables or disables the IDE controllers.	
Options	*Enabled*	*Disabled*

HDC Configure as

Description	Set hard disk controller configure type.	
Options	*IDE*	*RAID*
	AHCI	

Channel 1/2/3/4 Master

Description	Mapped automatically by the BIOS. You can make no changes here.

Video Configuration — Sub-menu

```
Render Standby                [Enabled]
Render Thermal Throttling     [Enabled]
IGD - Device2, Function1      [Enabled]
IGD - Pre-allocated Memory    [UMA = 64MB]
IGD - DVMT Size               [DVMT Max]
IGD  - Boot Type              [VBIOS Default]
IGD - LCD Panel Type          [1024x768 LVDS]
IGD - PAVP Mode               [Lite]
IGD - Gfx Low Power Mode      [Enabled]
```

Render Standby

Description	Check to enable render standby support.	
Options	*Enabled*	*Disabled*

Render Thermal Throttling

Description	This feature is applicable for Graphic SKUs only	
Options	*Enabled*	*Disabled*

IGD - Device2, Function1

Description	Enable/Disable function 1 of the internal graphics device by setting item to the desired value	
Options	*Enabled*	*Disabled*

IGD - Pre-allocated Memory

Description	Select the amount of pre-allocated memory that the Internal Graphics Device will use. Warning: Some feature may not be supported with 1MB pre-allocated memory.	
Options	*UMA = 32 MB*	*UMA = 64 MB*

IGD - DVMT Size

Description	Select the size of DVMT 3.0 that the Internal Graphics Device will use	
Options	*64 MB*	*128 MB*
	224MB	

IGD - Boot Type

Description	Select the Video Device that will be activated during POST	
Options	*VBIOS Default*	*CRT*
	LFP	*CRT+LFP*
	TV	*LFP-SDVO*
	EFP	*TV-SDVO*
	CRT+LFP-SDVO	*CRT+EFP*

IGD - LCD Panel Type		
Description	Select the panel used by the Internal Graphics Device	
Options	*640x480 LVDS*	*800x600 LVDS*
	1024x768 LVDS	*1280x1024 LVDS*
	1400x1050 LVDS1	*1400x1050 LVDS2*
	1600x1200 LVDS	

IGD - PAVP Mode		
Description	GMCH protected audio video path BIOS support	
Options	*Disabled*	*Lite*
	High	

IGD - Gfx Low Power Mode		
Description	Applicable for SFF only	
Options	*Enabled*	*Disabled*

USB Configuration — Sub-menu

```
USB Legacy               [Enabled]

EHCI 1                   [Enabled]
EHCI 2                   [Enabled]
UHCI 1                   [Enabled]
UHCI 2                   [Enabled]
UHCI 3                   [Enabled]
UHCI 4                   [Enabled]
UHCI 5                   [Enabled]
Pre-Port Control         [Disabled]

USB Pre-fetch Feature    [Enabled]
USB Pre-fetch Time       [2ms]
USB HC Alignment         [Enabled]
```

USB Legacy

Description	If this menu item is enabled it is possible to boot from USB devices and use a USB keyboard under DOS. Cannot be changed.	
Options	*Enabled*	

EHCI 1/2

Description	Enable/Disable EHCI 1/2.	
Options	*Enabled*	*Disabled*

UHCI 1/2/3/4/5

Description	Enable UHCI 1/2/3/4/5.	
Options	*Enabled*	*Disabled*

Pre-Port Control

Description	Enable/Disable the per port disable control override	
Options	*Enabled*	*Disabled*

USB Pre-fetch Feature

Description	Enable/Disable the USB pre-fetch Feature	
Options	*Enabled*	*Disabled*

USB Pre-fetch Time

Description	Select the USB pre-fetch time.	
Options	*2ms*	*4ms*

USB HC Alignment

Description	Enable/Disable the USB HC Alignment.	
Options	*Enabled*	*Disabled*

Chipset Configuration

```
Setup warning
Setting items on this screen to incorrect values may cause your system
to malfunction!
CRID                      [Enabled]
DMI Link ASPM Control     [Enabled]
Automatic ASPM            [Auto]
Manual:---------
ASPM L0s Support          [Disabled]
ASPM L0sL1 Support        [Disabled]
-----------------
VT-d                      [Enabled]
System Memory Frequency   [Auto]

>Memory Thermal Management
   TM Mode                [Disabled]
   TS on DIMM             [Disabled]
   TM lock                [Disabled]
```

CRID

Description	Enable or disable : Compatible Revision ID (CRID) / Stepping Revision ID (SRID)	
Options	*Enabled*	*Disabled*

DMI Link ASPM Control

Description	Enable or disable the control of Active State Power Management on both GMCH side and ICH8M side of the DMI Link.	
Options	*Enabled*	*Disabled*

Automatic ASPM

Description	Automatically or manually control the level of ASPM supported on the DMI Link.	
Options	*Auto*	*Manual*

ASPM L0s Support

Description	Control L0s Entry Support on the DMI Link	
Options	*Enabled*	*Disabled*

ASPM L0sL1 Support

Description	Control L0s and L1 Entry Support on the DMI Link	
Options	*Enabled*	*Disabled*

VT-d

Description	Check to enable VT-d function on MCH	
Options	*Enabled*	*Disabled*

System Memory Frequency		
Description	Determines the System Memory Frequency.	
Options	*Auto*	No change in System Memory Frequency.
	667MHz	System Memory Frequency fixed at 667MHz.
Memory Thermal Management		
Description	Configure Memory Thermal Management	
TM Mode		
Description	Select TM mode. Cannot be changed.	
Options	*Disabled*	
TS on DIMM		
Description	Enable or disable TS on DIMM. Cannot be changed.	
Options	*Disabled*	
TM Lock		
Description	Enable or disable TM Lock. Cannot be changed.	
Options	*Disabled*	

ACPI Table/Feature Control

```
FACP - C2 Latency Value  [Disabled]
FACP - C3 Latency Value  [Disabled]
FACP - RTC S4 Wakeup     [Enabled]
APIC - IO APIC Mode      [Enabled]
HPET - HPET Support      [Enabled
Enabled:-----
xBase Address select     [FED00000h]
```

FACP - C2 Latency Value

Description	Value only for ACPI. Select the value for the P_LVL2_LAT field found in the FACP Table where: 1 = C2 Enabled, 101 = C2 Disabled	
Options	*Enabled*	*Disabled*

FACP - C3 Latency Value

Description	Value only for ACPI. Select the value for the P_LVL3_LAT field found in the FACP Table where: 57 = C3 Enabled, 1001 = C3 Disabled	
Options	*Enabled*	*Disabled*

FACP - RTC S4 Wakeup

Description	Value only for ACPI. Enable/Disable for S4 Wakeup from RTC	
Options	*Enabled*	*Disabled*

APIC - IO APIC Mode

Description	This item is valid only for WIN2k and WINXP.Also, a fresh install of the OS must occur when APIC Mode is desired.Test the IO ACPI by setting item to Enable.The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in ICH4M.	
Options	*Enabled*	*Disabled*

HPET - HPET Support

Description	High Performance Event Timer Support in Windows XP. If this feature is enabled, the HPET table will be added into the ACPI Tables.	
Options	*Enabled*	*Disabled*

Base Address Select

Description	Memory address ranges of High Performance Event Timer. Only available if HPET support is enabled.	
Options	FED00000h	FED10000h
	FED20000h	FED30000h

PCI Express Root Port 1/2/3/4/5/6 Settings

```
PCI Express Root Port 1 [Enabled]
VC1 Enable              [Disabled]
Auto:
xVC1/TC Mapping         [TC7]
ASPM                    [Enabled]
Automatic ASMP          [Auto]
Manual: ---
xASPM LOs               [Root&Endpoint Ports]
xASPM L1                [Enabled]

URR                     [Disabled]
FER                     [Disabled]
NFER                    [Disabled]
CER                     [Disabled]
CTO                     [Disabled]
SEFE                    [Disabled]
SENFE                   [Disabled]
SECE                    [Disabled]
PME Interrupt           [Disabled]
PME SCI                 [Disabled]
Hot Plug SCI            [Disabled]
```

PCI Express Root Port 1/2/3/4/5/6

Description	If PCI Express Root Port 1 is disabled, PCI Express Root Ports 2 to 6 will also be disabled.	
Options	*Enabled*	*Disabled*

VC1 Enable

Description	Enable or disable Virtual Channel 1.	
Options	*Disabled*	*Auto*

VC1/TC Mapping

Description	Set Virtual Channel 1 (VC1) to Traffic Class (TC) Mappings.	
Options	*Disabled*	*Auto*

ASPM

Description	Enable ASPM settings.	
Options	*Enabled*	*Disabled*

Automatic ASPM

Description	Automatically enable ASPM based on reported capabilities and known issues.	
Options	*Auto*	*Manual*

ASPM LOs		
Description	Enable PCIe ASPM LOs. Only available if Automatic ASPM is set to Manual.	
Options	*Root&Endpoint Ports*	*Disabled*
	Root Port only	*Endpoint Port only*
ASPM L1		
Description	Enable PCIe ASPM L1. Only available if Automatic ASPM is set to Manual.	
Options	*Enabled*	*Disabled*
URR		
Description	Enable or disable PCI Express Unsupported Request Reporting.	
Options	*Enabled*	*Disabled*
FER		
Description	Enable or disable PCI Express Device Fatal Error Reporting.	
Options	*Enabled*	*Disabled*
NFER		
Description	Enable or disable Device Non-Fatal Error Reporting.	
Options	*Enabled*	*Disabled*
CER		
Description	Enable or disable PCI Express Device Correctable Error Reporting.	
Options	*Enabled*	*Disabled*
CTO		
Description	Enable or disable PCI Express Completion Timer.	
Options	*Enabled*	*Disabled*
SEFE		
Description	Enable or disable Root PCI Express System Error on Fatal Error.	
Options	*Enabled*	*Disabled*
SENFE		
Description	Enable or disable Root PCI Express System Error on Non-Fatal Error.	
Options	*Enabled*	*Disabled*

SECE		
Description	Enable or disable Root PCI Express System Error on Correctable Error.	
Options	*Enabled*	*Disabled*
PME Interrupt		
Description	Enable or disable Root PCI Express PME Interrupt.	
Options	*Enabled*	*Disabled*
PME SCI		
Description	Enable or disable PME SCI.	
Options	*Enabled*	*Disabled*
Hot Plug SCI		
Description	Enable or disable PCI Express Hot Plug SCI.	
Options	*Enabled*	*Disabled*

3.3 Security

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
TPM Status			Not Installed			
TPM Operation			[No Operation]			
Supervisor Password			[Installed/Not Installed]			
User Password			[Installed/Not Installed]			
Set Supervisor Password						
Power on password			[Disabled]			
User Access level			[View Only]			
Set User Password						
Set all Hdd Pasword						
F1 Help		↑↓ Select Item		F5/F6 Change Values		F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Sub-menu		F10 Save and Exit

TPM Status

Description	TPM (Trusted Platform Module) Status. Not supported on the XM2.
Options	*Not installed*

TPM Operation

Description	TPM (Trusted Platform Module) Operation. Not supported on the XM2.
Options	*No operation*

Supervisor Password

Description	Shows whether a supervisor password has been entered.

User Password

Description	Shows whether a user password has been entered.

Set Supervisor Password

Description	Enter and confirm the supervisor password under this menu item. To delete the password enter an empty password.

Power On Password

Description	Select when the password has to be entered.	
Options	*Enabled*	The password has to be entered when the system starts.
	Disabled	The password has to be entered when changing to the setup menu.

User Access Level

Description	Set the User Access Level.	
Options	*View Only*	Access to InsydeH2O Setup allowed but the fields cannot be changed.
	Full	Any field can be changed except the Supervisor password.
	Limited	Only limited fields can be changed.

Set User Password

Description	Enter and confirm the user password under this menu item.

Set all Hdd Password

Description	Enter and confirm the password for locking all gard disks under this menu item To delete the password enter an empty password.

3.4 Power

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
>Advanced CPU Control						
>Platform Power Management						
>Break Event						
ACPI S3			[Enabled]			
Wake on PME			[Disabled]			
Auto Wake on S5			[Disabled]			
F1 Help		↑↓ Select Item		F5/F6 Change Values		F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Sub-menu		F10 Save and Exit

Advanced CPU Control – Sub-Menu

```
TXT                         [Disable]
P-States(IST)               [Enabled]
Boot Performance Mode       [Max Performance]
Thermal Mode                [Disabled]
CMP Support                 [Auto]
Use XD Capability           [Enabled]
VT Support                  [Disabled]
SMRR Support                [Auto]
C-States                    [Enabled]
Enhanced C-States           [Enabled]
C-State Pop Up Mode         [Enabled]
C-State Pop Down Mode       [Enabled]
C4 Exit Timing Mode         [Fast]
DeepC4                      [Enabled]
Hard C4E                    [Enabled]
Enable C6                   [Enabled]
EMTTM                       [Enabled]
Bi-directional PROCHOT#     [Enabled]
Dynamic FSB Switching       [Enabled]
Turbo Mode                  [Enabled]
ACPI 3.0 T-States           [Disabled]
DTS                         [Enabled]
DTS Calibration             [Enabled]

>Thermal Trip Points Setting
  Throttle On Temperature  [40øC]
```

TXT

Description	Enables utilization of additional hardware capabilities provided by Intel Trusted Execution Technology; changes require a full power cycle to take effect.	
Options	*Enabled*	*Disabled*

P-States (IST)

Description	Enable processor performance states (P-States).	
Options	*Enabled*	*Disabled*

Boot Performance Mode

Description	Select the performance state that BIOS will set before OS hand-off.	
Options	*Max Performance*	*Max Battery*

Thermal Mode

Description	Select the Thermal Mode.	
Options	*Disabled*	*TM1*
	TM2	*TM1 and TM2*

CMP Support		
Description	Enable or disable core multi processing.	
Options	*Auto*	*Disabled*
Use XD Capability		
Description	Enable or disable XD capability.	
Options	*Enabled*	*Disabled*
VT Support		
Description	Enable or disable Vanderpool technology.	
Options	*Enabled*	*Disabled*
SMRR Support		
Description	Enable or disable SMRR Support.	
Options	*Auto*	*Disabled*
C-States		
Description	Enable processor idle power saving states (C-States).	
Options	*Enabled*	*Disabled*
Enhanced C-States		
Description	Enable P-State transitions to occur in combination with C-States.	
Options	*Enabled*	*Disabled*
C-State Pop Up Mode		
Description	If enabled and ICH abserves a bus master request, it will take the system from C3/C4 to C2 and auto enable bus masters. If disabled, bus master traffic is a break event and ICH will attempt to return to C0 state.	
Options	*Enabled*	*Disabled*
C-State Pop Down Mode		
Description	If enabled and ICH abserves no bus master requests, it can return to the previous C3/C4 state. If disabled, ICH will not attempt to automatically return to the previous C3/C4 state.	
Options	*Enabled*	*Disabled*
C4 Exit Timing Mode		
Description	This option controls a programmable time for the CPU voltage to stabilize when exiting from a C4 state.	
Options	*Fast*	*Default*
	Slow	*Force Slow*

DeepC4		
Description	Enable Deep C4 with L2 Cache disable instead of C4.	
Options	*Enabled*	*Disabled*
Hard C4E		
Description	Enable P-State transitions to minimum state on C4E.	
Options	*Enabled*	*Disabled*
Enable C6		
Description	Enables or disables the C6 state (Deep Power Down Technology).	
Options	*Enabled*	*Disabled*
EMTTM		
Description	Enable processor Enhanced Multi Threaded Thermal Monitoring (requires GV3).	
Options	*Enabled*	*Disabled*
Bi-directional PROCHOT#		
Description	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-directional is enabled, external agents can drive PROCHOT# to throttle.	
Options	*Enabled*	*Disabled*
Dynamic FSB Switching		
Description	Enable or disable processor Dynamic FSB Frequency Switching (Bus GV)	
Options	*Enabled*	*Disabled*
Turbo Mode		
Description	Enable processor Turbo Mode (requires EMTTM enabled too).	
Options	*Enabled*	*Disabled*
ACPI 3.0 T-States		
Description	Enable or disable ACPI 3.0 T-States	
Options	*Enabled*	*Disabled*
DTS		
Description	Enables CPU Digital Thermal Sensor function.	
Options	*Enabled*	*Disabled*
DTS Calibration		
Description	Enables Calibration function.	
Options	*Enabled*	*Disabled*

>Thermal Trip Points Setting

Throttle On Temperature

Description	Set the CPU temperature point at which the throttle is activated.	
Options	*40°C*	*45°C*
	50°C	*55°C*
	60°C	*65°C*
	70°C	*75°C*
	80°C	*85°C*
	90°C	

Platform Power Management – Sub-Menu

```
PCI Clock Run              [Enabled]
```

PCI Clock Run

Description	If Enabled,the CLKRUN# Logic will stop the PCI Clocks.	
Options	*Enabled*	*Disabled*

Break Event – Sub-Menu

```
Storage Break Event        [Disabled]
PCIE Break Event           [Disabled]
PCI Break Event            [Disabled]
EHCI Break Event           [Disabled]
UHCI Break Event           [Disabled]
HDA Break Event            [Disabled]
```

Storage Break Event

Description	If Enabled, Parallel IDE or Serial ATA master activity will cause BM_STS to be set and will cause a break from C3/C4.	
Options	*Enabled*	*Disabled*

PCIE Break Event

Description	If Enabled, PCI Express master activity will cause BM_STS to be set and will cause a break from C3/C4.	
Options	*Enabled*	*Disabled*

PCI Break Event

Description	If Enabled, PCI master activity will cause BM_STS to be set and will cause a break from C3/C4.	
Options	*Enabled*	*Disabled*

EHCI Break Event

Description	If Enabled, EHCI master activity will cause BM_STS to be set and will cause a break from C3/C4.	
Options	*Enabled*	*Disabled*

UHCI Break Event

Description	If Enabled, UHCI master activity will cause BM_STS to be set and will cause a break from C3/C4.	
Options	*Enabled*	*Disabled*

HDA Break Event

Description	If Enabled, Intel High Definition Audio master activity will cause BM_STS to be set and will cause a break from C3/C4.	
Options	*Enabled*	*Disabled*

ACPI S3

Description	Enable/Disable ACPI S1/S3 Sleep state	
Options	*Enabled*	*Disabled*

Wake on PME

Description	Determines the action taken when the system power is off and a PCI Power Management Enable wake up event occurs.	
Options	*Enabled*	*Disabled*

Auto Wake on S5

Description	Auto wake on S5, By Day of Month or Fixed time of every day	
Options	*Disabled*	*By every day*
	By day of month	

3.5 Boot

InsydeH2O Setup Utility					Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit
UEFI Boot			[Enabled]		
Quick Boot			[Enabled]		
Quiet Boot			[Enabled]		
PXE Boot to LAN			[Disabled]		
ACPI Selection			[ACPI 3.0]		
USB Boot			[Enabled]		
>EFI					
>Legacy					
F1 Help		↑↓ Select Item		F5/F6 Change Values	F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Sub-menu	F10 Save and Exit

UEFI Boot

Description	Enable/Disable UEFI Boot Function	
Options	*Enabled*	*Disabled*

Quick Boot

Description	Allows InsydeH2O to skip certain tests while booting. This will decrease the time needed to boot the system.	
Options	*Enabled*	*Disabled*

Quiet Boot

Description	Disables or enables booting in Text Mode	
Options	*Enabled*	*Disabled*

PXE Boot to LAN

Description	Disables or enables PXE boot to LAN.	
Options	*Enabled*	*Disabled*

ACPI Selection

Description	Select booting to Acpi3.0/Acpi1.0B	
Options	Acpi3.0/	Acpi1.0B

USB Boot

Description	Disables or enables booting to USB boot devices.	
Options	*Enabled*	*Disabled*

EFI

Description	Prepared for future implementations.

Legacy – Sub-Menu

```
Boot Device Priority
> Normal Boot Menu          [Normal/Advance]

Normal                          Advance

> Boot Type Order               SanDisk Cruzer Micro

  Floppy Drive
  Hard Disk Drive
  CD/DVD-ROM Drive
  USB
  Others


> Hard Disk Drive
  SanDisk Cruzer Micro
```

Normal Boot Menu		
Description	Selects the type of boot order	
Options	*Normal*	Sub-menu Boot Type Order: Under this menu option it is possible to select the boot order of device groups (e.g. Hard Disk before Floppy Drive). Sub-menu USB: Under this menu option it is possible to select the boot order of single devices within a device group, e.g. USB-HDD before SATA-HDD
	Advance	Under this menu option there are no device groups. The single devices are listed and can be moved to select the boot order, e.g.: SATA-HDD1 USB-Floppy USB-DVD-DRIVE SATA-HDD2

3.6 Exit

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
Exit Saving Changes						
Save Change Without Exit						
Exit Discarding Changes						
Load Optimal Defaults						
Load Custom Defaults						
Save Custom Defaults						
Discard Changes						
F1 Help		↑↓ Select Item		F5/F6 Change Values		F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Sub-menu		F10 Save and Exit

3.6.1 Exit Saving Changes

Exit system setup and save your changes.

3.6.2 Save Change Without Exit

Save your changes without exiting the system.

3.6.3 Exit Discarding Changes

Exit system setup without saving your changes.

3.6.4 Load Optimal Defaults

If this option is selected, a verified factory setup is loaded.

On the first BIOS setup configuration, this loads safe values for setup, which make the board boot up.

3.6.5 Load Custom Defaults

If this option is selected the custom defaults that have been saved in a former session with Save Custom Defaults (see Chapter 3.6.6 Save Custom Defaults) are loaded.

3.6.6 Save Custom Defaults

Save custom defaults.

3.6.7 Discard Changes

Discard changes.

4 Organization of the Board

4.1 Memory Mappings

4.1.1 Processor View of the Memory Map

The memory map is allocated dynamically and may vary depending on the system configuration.

Table 9. *Memory map – processor view*

CPU Address Range	Description
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	VGA Display Controller
0x80000000-0xFEBFFFFF	PCI bus
0x80000000-0xFEBFFFFF	Standard VGA Graphics Adapter
0x96500000-0x965FFFFF	PCI standard PCI-to-PCI bridge
0x96500000-0x965FFFFF	Ethernet Controller
0x96520000-0x96523FFF	Ethernet Controller
0x90000000-0x903FFFFF	Standard VGA Graphics Adapter
0x93400000-0x934FFFFF	Video Controller
0x96605400-0x966057FF	Standard Enhanced PCI to USB Host Controller
0x96600000-0x96603FFF	Microsoft UAA Bus Driver for High Definition Audio
0x95500000-0x964FFFFF	PCI standard PCI-to-PCI bridge
0x90400000-0x913FFFFF	PCI standard PCI-to-PCI bridge
0x94500000-0x954FFFFF	PCI standard PCI-to-PCI bridge
0x94500000-0x954FFFFF	Ethernet Controller
0x91400000-0x923FFFFF	PCI standard PCI-to-PCI bridge
0x94520000-0x94523FFF	Ethernet Controller
0x93500000-0x944FFFFF	PCI standard PCI-to-PCI bridge
0x93500000-0x944FFFFF	Ethernet Controller
0x92400000-0x933FFFFF	PCI standard PCI-to-PCI bridge
0x93520000-0x93523FFF	Ethernet Controller
0x96605000-0x966053FF	Standard Enhanced PCI to USB Host Controller
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED13FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources
0xFEC00000-0xFEC00FFF	Motherboard resources

CPU Address Range	Description
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED40000-0xFED44FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEE00FFF	Motherboard resources
0xFED00000-0xFED003FF	High precision event timer
0xFF800000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device
0x96605800-0x966058FF	SM Bus Controller
0x96604000-0x96604FFF	PCI Data Acquisition and Signal Processing Controller

4.1.2 I/O Memory Map

Table 10. *Memory map - I/O*

Address Range	Description
0x00000000-0x00000CF7	PCI bus
0x00000000-0x00000CF7	Direct memory access controller
0x00000D00-0x0000FFFF	PCI bus
0x00005000-0x00005FFF	PCI standard PCI-to-PCI bridge
0x00005000-0x00005FFF	Ethernet Controller
0x00006140-0x00006147	Standard VGA Graphics Adapter
0x000060C0-0x000060DF	Standard Universal PCI to USB Host Controller
0x000060A0-0x000060BF	Standard Universal PCI to USB Host Controller
0x00004000-0x00004FFF	PCI standard PCI-to-PCI bridge
0x00003000-0x00003FFF	PCI standard PCI-to-PCI bridge
0x00003000-0x00003FFF	Ethernet Controller
0x00002000-0x00002FFF	PCI standard PCI-to-PCI bridge
0x00002000-0x00002FFF	Ethernet Controller
0x00006080-0x0000609F	Standard Universal PCI to USB Host Controller
0x00006060-0x0000607F	Standard Universal PCI to USB Host Controller
0x00006040-0x0000605F	Standard Universal PCI to USB Host Controller
0x00006020-0x0000603F	Standard Universal PCI to USB Host Controller
0x00000061-0x00000061	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000063-0x00000063	Motherboard resources

Address Range	Description
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000600-0x0000060F	Motherboard resources
0x00000610-0x00000610	Motherboard resources
0x00000800-0x0000080F	Motherboard resources
0x00000810-0x00000817	Motherboard resources
0x00000820-0x00000823	Motherboard resources
0x00000400-0x0000047F	Motherboard resources
0x00000500-0x0000053F	Motherboard resources
0x00000081-0x00000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x000000F0-0x000000F0	Numeric data processor
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x00006138-0x0000613F	Standard Dual Channel PCI IDE Controller
0x00006154-0x00006157	Standard Dual Channel PCI IDE Controller
0x00006130-0x00006137	Standard Dual Channel PCI IDE Controller
0x00006150-0x00006153	Standard Dual Channel PCI IDE Controller
0x00006110-0x0000611F	Standard Dual Channel PCI IDE Controller

Address Range	Description
0x00006100-0x0000610F	Standard Dual Channel PCI IDE Controller
0x00006000-0x0000601	FSM Bus Controller
0x00006128-0x0000612F	Standard Dual Channel PCI IDE Controller
0x0000614C-0x0000614F	Standard Dual Channel PCI IDE Controller
0x00006120-0x00006127	Standard Dual Channel PCI IDE Controller
0x00006148-0x0000614B	Standard Dual Channel PCI IDE Controller
0x000060F0-0x000060FF	Standard Dual Channel PCI IDE Controller
0x000060E0-0x000060EF	Standard Dual Channel PCI IDE Controller
0x000003B0-0x000003BB	VGA Display Controller
0x000003C0-0x000003DF	VGA Display Controller
0x000001CE-0x000001CF	VGA Display Controller
0x000002E8-0x000002EF	VGA Display Controller

4.2 PCI Devices

Table 11. *PCI Devices*

Bus	Device Number	Device Function	Vendor ID	Device ID	Class	Function
0	0x00	0x0	0x8086	0x2A40	Host Bridge	Intel GS45 Chipset Processor to I/O Controller
	0x01	0x0	0x8086	0x2A41	PCI Bridge (0-1)	Intel GS45 Chipset PCIe Port Port 1
	0x02	0x0	0x8086	0x2A42	VGA Controller	Intel GS45 Chipset Integrated Graphics Controller 1
	0x02	0x1	0x8086	0x2A43	Non VGA Controller	Intel GS45 Chipset Integrated Graphics Controller 2
	0x26	0x0	0x8086	0x2937	UHCI USB Controller	Intel 82801IEM (ICH9M-E) USB UHCI Controller #4
	0x26	0x1	0x8086	0x2938	UHCI USB Controller	Intel 82801IEM (ICH9M-E) USB UHCI Controller #5
	0x26	0x7	0x8086	0x293C	EHCI USB Controller	Intel 82801IEM (ICH9M-E) USB EHCI Controller #2
	0x27	0x0	0x8086	0x293E	High Def Audio	Intel 82801IEM (ICH9M-E) HD Audio Controller
	0x28	0x0	0x8086	0x2940	PCI Bridge (0-2)	Intel 82801IEM (ICH9M-E) PCIe Port 1
	0x28	0x4	0x8086	0x2948	PCI Bridge (0-3)	Intel 82801IEM (ICH9M-E) PCIe Port 5
	0x28	0x5	0x8086	0x294A	PCI Bridge (0-4)	Intel 82801IEM (ICH9M-E) PCIe Port 6
	0x29	0x0	0x8086	0x2934	UHCI USB Controller	Intel 82801IEM (ICH9M-E) USB UHCI Controller #1
	0x29	0x1	0x8086	0x2935	UHCI USB Controller	Intel 82801IEM (ICH9M-E) USB UHCI Controller #2
	0x29	0x2	0x8086	0x2936	UHCI USB Controller	Intel 82801IEM (ICH9M-E) USB UHCI Controller #3
	0x29	0x3	0x8086	0x2939	UHCI USB Controller	Intel 82801IEM (ICH9M-E) USB UHCI Controller #6
	0x29	0x7	0x8086	0x293A	EHCI USB Controller	Intel 82801IEM (ICH9M-E) USB EHCI Controller #1
	0x30	0x0	0x8086	0x2448	PCI Subtractive (0-5)	Intel 82801IEM (ICH9M-E) Hub Interface to PCI Bridge
	0x31	0x0	0x8086	0x2917	ISA Bridge	Intel 82801IEM (ICH9M-E) LPC Interface Controller
	0x31	0x2	0x8086	0x2928	SATA Controller	Intel 82801IEM (ICH9M-E) 2 port SATA I/O Controller 1 cc=EIDE
	0x31	0x3	0x8086	0x2930	SMBus Controller	Intel 82801IEM (ICH9M-E) SMBus Controller
	0x31	0x5	0x8086	0x292D	Disk Controller	Intel 82801IEM (ICH9M-E) 2 port SATA I/O Controller 2 cc=EIDE
	0x31	0x6	0x8086	0x2932	Other DPIO Module	Intel 82801IEM (ICH9M-E) Thermal Subsystem

Bus	Device Number	Device Function	Vendor ID	Device ID	Class	Function
1	0x00	0x0	0x8086	0x10D3	Ethernet Controller	Intel 82574L Gigabit Network Connection
3	0x00	0x0	0x8086	0x10D3	Ethernet Controller	Intel 82574L Gigabit Network Connection
4	0x00	0x0	0x8086	0x10D3	Ethernet Controller	Intel 82574L Gigabit Network Connection

4.3 SMBus Devices

Table 12. *SMBus devices*

Address[1]	Function
0x9A / 0x9B	Board controller
0x98	Temperature sensor
0xA0	SPD of SO-DIMM (memory channel A)
0x60	Protect register
0xA4	SPD of SO-DIMM (memory channel B)
0x64	Protect register
0xAE	ID EEPROM
0x6E	Protect register
0xD2 / 0xD3	Clock generator

[1] The first address is for write command, the second for read command

4.4 Interrupt Mapping

Table 13. *Interrupt Mapping*

Interrupt	Function
IRQ 9	Microsoft ACPI-Compliant System
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 16	Standard Universal PCI to USB Host Controller
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 16	Standard Universal PCI to USB Host Controller
IRQ 11	Ethernet Controller
IRQ 11	Standard VGA Graphics Adapter
IRQ 11	Microsoft UAA Bus Driver for High Definition Audio
IRQ 11	Ethernet Controller
IRQ 11	Ethernet Controller
IRQ 11	SM Bus Controller
IRQ 11	PCI Data Acquisition and Signal Processing Controller
IRQ 21	Standard Universal PCI to USB Host Controller

Interrupt	Function
IRQ 19	Standard Enhanced PCI to USB Host Controller
IRQ 19	Standard Universal PCI to USB Host Controller
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 17	PCI standard PCI-to-PCI bridge
IRQ 17	PCI standard PCI-to-PCI bridge
IRQ 23	Standard Universal PCI to USB Host Controller
IRQ 23	Standard Enhanced PCI to USB Host Controller
IRQ 18	Standard Universal PCI to USB Host Controller
IRQ 0	High precision event timer
IRQ 8	High precision event timer
IRQ 13	Numeric data processor

5 Appendix

5.1 Literature and Web Resources

- XM2 data sheet with up-to-date information and documentation:
  www.men.de/products/15xm02-.html
- XC1 data sheet with up-to-date information and documentation:
  www.men.de

5.1.1 CPU

- Intel Processors
  www.intel.com

5.1.2 SATA

- Serial ATA International Organization (SATA-IO)
  www.serialata.org

5.1.3 USB

- USB:
  Universal Serial Bus Specification Revision 1.0; 1996; Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom
  www.usb.org

5.1.4 Ethernet

- ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE
  www.ieee.org
- Charles Spurgeon's Ethernet Web Site
  Extensive information about Ethernet (IEEE 802.3) local area network (LAN) technology.
  www.ethermanage.com/ethernet/
- InterOperability Laboratory, University of New Hampshire
  This page covers general Ethernet technology.
  www.iol.unh.edu/services/testing/ethernet/training/

5.1.5 HD Audio

- Intel High Definition Audio:
  www.intel.com/design/chipsets/hdaudio.htm

5.1.6 PCI Express

- PCI Express Base Specification, Revision 1.0
  April 29, 2002
  PCI Special Interest Group
  www.pcisig.com

5.2 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the XM2. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 5. *Labels giving the board's article number, revision and serial number*